

Gauging the Capability of Artificial Intelligence Chatbot Tools to Answer Textbook Coursework Exercises in Circuit Design Education

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Abstract—Powerful chatbots, based on intensively-trained large language models, have recently become available for consumer use. The ability of such chatbots to provide credible textual responses to sophisticated engineering problems has been demonstrated in various subfields. This paper seeks to gauge the extent to which such a chatbot can be prompted to complete a set of homework and project exercises for university-level courses in analog, digital, mixed-signal, and signal processing classes. The purpose of this paper is to delineate and clearly articulate the present capabilities of artificial intelligence tools to complete coursework tasks across the field of circuit theory. Building on these research findings, this paper suggests practical ways to mitigate artificial intelligence chatbot tools’ disruption to academic integrity and genuine learning in universities.

I. INTRODUCTION

Since late 2022, consumer Large Language Models (LLMs) have emerged as a popular computer technology widely used in everyday life [1]. The availability of these powerful tools raises concerns across multiple fields, including engineering education [2]. Specifically, the impressive capabilities of the latest generation of chatbot tools have sparked considerable worry that students might use LLMs to complete assessments dishonestly within university engineering modules [3], [4].

Modern LLM agents primarily function as “*text-in, text-out*” tools, accepting arbitrary prompts of unstructured prose as input and then returning textual responses, which may include computer code or mathematical equations. The most advanced models, such as ChatGPT-4o¹ and Google Gemini², have developed the ability to further interact with the real world via live video and audio, further expanding the number of use-cases, simplifying their use and lowering the entry barrier. Additionally, LLMs are continuously broadening and deepening their knowledge across various domains at a fast pace, thanks to the increasing scale of training datasets and the amount of model parameters considered. There is a growing literature that documenting their nascent capabilities and the consequent implications for teaching, learning and assessment in universities [4], [5].

Assessment activities in university circuit design education involves elements of abstract thinking, analysis, and software-

assisted simulations of electrical circuits and systems, often provided as take-home homework questions or problem sheets.

In this paper, we document *Claude 3.5 Sonnet*’s³ ability to solve homework-style circuit problems, ranging from single-transistor to system-level design problems. This particular model was selected due to its strong logical reasoning and mathematical capabilities [6]. Building from the observed results, we conclude with suggestions for a practical approach to integrate LLMs into circuit design courses.

II. METHODOLOGY

This study aims to investigate the integrity and robustness of extant circuit design assignments across analog and mixed-signal domains. We investigate how well Anthropic’s *Claude 3.5 Sonnet* can handle different forms of continuous assessment such as homework assignments, design labs and projects. This audit is intended to identify the current limits of LLM capabilities (as of late Summer 2024) and to indicate how coursework assessments should evolve in this field of engineering and beyond.

A. LLM Guided Homework Solutions

In this case, the homework-style assignments used to evaluate LLM performance are derived from well-established educational examples found in both academic and industry-leading literature, without any solutions publicly available online. Sample questions are sourced from three well-known textbooks:

- B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY: McGraw-Hill Professional, Jan. 2016
- P. J. Ashenden, *Digital design (Verilog)*. London, England: Morgan Kaufmann, Oct. 2007
- M. J. M. Pelgrom, *Analog-to-digital conversion*, en, 4th ed. Cham, Switzerland: Springer Nature, Mar. 2022

This approach enhances the likelihood that the problems presented are novel to the LLM agent, thereby providing a more accurate evaluation of its true capabilities. An example problem, 7.5 [7], is shown in detail in Fig. 2. The complete summary listing of the problems, and the provided solutions, is given in Tables I, II and III. These tables group tasks by difficulty, providing domains and complexity keywords to provide more context about each problem. A full archive of the sample problems and their solutions is available at the online repository Figshare⁴.

The process used to assess the homework solving capabilities of *Claude* is described in Fig. 1. To ensure an unbiased assessment, the model is initially presented with a problem

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¹<https://openai.com/index/hello-gpt-4o/>

²<https://deepmind.google/technologies/gemini/pro/>

³<https://www.anthropic.com/news/claude-3-5-sonnet>

⁴<https://figshare.com/s/88803f670a3f622d97d0>

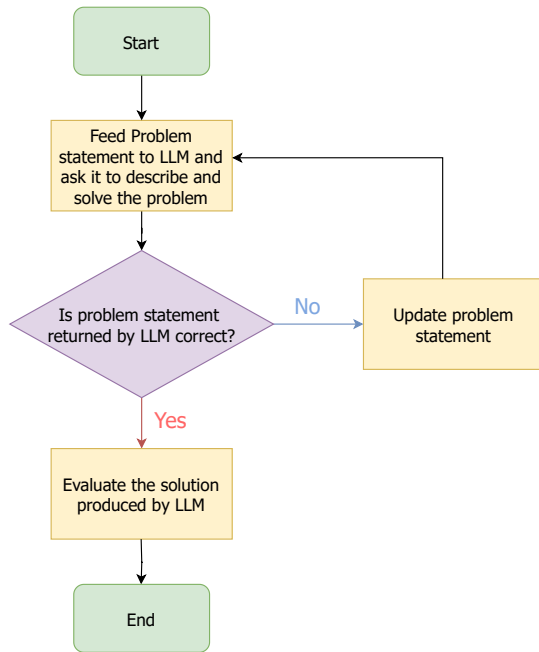


Figure 1. This flowchart documents the prompting procedure used in gauging the chatbot's capabilities. The approach documented here mimics what a dishonest student might do; iterating until the problem is properly taken in by the chatbot, and then plagiarising its answer as a solution to a homework problem.

statement and explicitly instructed to meticulously describe the task. If the LLM returns an erroneous problem description, explicit corrections are made. This mimics how a dishonest student might proactively interact with a chatbot to maximise their chances of eliciting a quality response.

This step is crucial to allow the LLM's problem-solving abilities to be assessed explicitly, while minimizing input processing errors. Subsequently, the LLM is asked to solve the problem based on its own description. The solutions are then evaluated by an expert in the relevant field, who assesses the quality of the output. In some cases, clarifying questions are introduced to obtain more detailed responses from the system. A notional letter grade is assigned for each problem, as a high-level indicator of the LLM's performance against a typical academic rubric.

B. Lab and Project-based Assessment

In order to further assess the capabilities of LLMs and identify the limits of AI today, a more ambitious project was also tested. A basic lab project assignment, which includes the design, optimisation and evaluation of a 2-stage differential OPAMP is used to assess the performance of the system when dealing with larger scale and more open-ended problems.

Feedback between the LLM chatbot and LTspice *Analog Design Environment* (ADE) is introduced so that the system can correct itself.

At first, the LLM is tasked to implement the netlist of the circuit and a corresponding testbench from the image shown in Fig. 3. Afterwards, the LLM is used to optimise the design parameters to meet the required circuit specifications.

PROMPT: 7.5 Calculate the input-referred thermal noise voltage of the circuit in Fig. 7.70. When approaching this problem act as follows:
 1. Carefully inspect the circuit diagram and transcribe it to a verbal net list. You are a meticulous data entry specialist and I will pay you for accurate transcription
 2. Then once you have the netlist you must become a circuit analysis expert and solve the problem

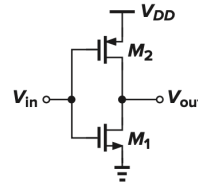


Figure 7.70

RESPONSE: Thank you for providing this circuit diagram. I'll approach this problem as you've requested.

1. Circuit transcription (netlist):

- Power supply VDD connected to the source of transistor M2
- Transistor M2: PMOS, drain connected to Vout, source connected to VDD, gate connected to Vin
- Transistor M1: NMOS, drain connected to Vout, source connected to ground, gate connected to Vin
- Input voltage Vin connected to gates of both M1 and M2
- Output voltage Vout taken from the connected drains of M1 and M2

2. Circuit analysis for input-referred thermal noise voltage: To calculate the input-referred thermal noise voltage, we need to consider the thermal noise contributions from both transistors M1 and M2.

For MOSFETs in saturation, the thermal noise power spectral density is given by:

$$S_{id} = 4kT\gamma gm$$

Where: k is Boltzmann's constant T is absolute temperature γ is the noise factor (typically $2/3$ for long-channel devices) gm is the transconductance of the transistor

The input-referred noise voltage is found by referring the output noise back to the input by dividing by the square of the small-signal voltage gain (A_v^2).

For this inverter configuration:

1. Output noise: $S_{vout} = S_{id1}/(gm1 + gm2)^2 + S_{id2}/(gm1 + gm2)^2$
2. Small-signal voltage gain: $A_v = -(gm1 + gm2)/(gds1 + gds2)$
3. Input-referred noise: $S_{vin} = S_{vout}/A_v^2$

Substituting and simplifying:

$$S_{vin} = [4kT\gamma(gm1 + gm2)]/(gm1 + gm2)^2 = 4kT\gamma/(gm1 + gm2)$$

The input-referred thermal noise voltage (RMS) over a bandwidth Δf is: $V_{n,in} = \text{sqrt}(4kT\gamma\Delta f/(gm1 + gm2))$

This is the final expression for the input-referred thermal noise voltage of the circuit. To get a numerical value, you would need to know or assume values for temperature, bandwidth, and the transconductances of M1 and M2.

REVIEW: Correct metastable state solution
 Grade: A

Figure 2. Example of a prompting session with Claude 3.5 Sonnet, showing the inputting of a question and the returned solution

Table I.
SUMMARY OF EASIER PROBLEMS ATTEMPTED BY CLAUDE 3.5 SONNET

Problem	Technical Topic and Task	Domain	Grade	Comments
Easier Problems				
1.5 [8]	Design combinational logic from textual description	Digital	A	✓ Correct Interpretation of Desired Logic
2.2 [7]	Find small signal parameters of a circuit in the given operating point (OP)	AC	A	✓ Correct for NMOS. ✓ Correct for PMOS.
2.3 [7]	Derive small signal relationship between intrinsic gain $g_m r_o$ and W and L of transistor	AC	A	✓ Correct small signal analysis and equations handling.
2.4 [7]	Plot I_D vs V_{GS} with drain-source V_{DS} and bulk-source V_{BS} voltages as parameters	DC	A	✓ Correct solution of DC sweep. ✓ Correct identification of different operating modes.
2.5 [7]	Sketch I_D and transconductance g_m as a function of external voltage	AC DC	A	✓ Correct I_D calculation. ✓ Correct g_m calculation.
2.7 [7]	Sketch I_D and g_m as a function of external voltage	AC DC	A	✓ Correct I_D calculation depending on V_{GS} . ✓ Correct g_m calculation depending on V_{GS} .
2.9 [7]	Find transient response of a circuit with a capacitor and CMOS	Transient	A	✓ Correct transient analysis for 4 different circuits.
7.5 [7]	Noise Analysis in digital inverter gate	Noise	A	✓ Correct noise analysis in metastable state.
6.6 [9]	Static Random Access Memory (SRAM) input offset estimate	Mismatch	A	✓ SRAM input offset estimate due to mismatch is correct.
7.12 [9]	Design of filters for a specific frequency response	AC	A	✓ Correct analog filter. ✓ Correct digital filter.
7.18 [9]	Spectrum and oversampling analysis	AC	A	✓ SNR calculation is correct. ✓ Spectrum is correct.
6.8 [9]	Design of current source to minimise mismatch	DC Mismatch	B	✓ Correct estimate of mismatch. × Area spec is not met.
2.1 [7]	Plot drain current I_D vs gate-source voltage V_{GS}	DC	C	✓ Correct saturation state plot. × Failed to include an OFF state in the plot.
2.5 [8]	Truth table from digital logic gate diagram	Digital	C	× Failed to correctly identify XOR gate in diagram. ✓ Correct Truth table construction.

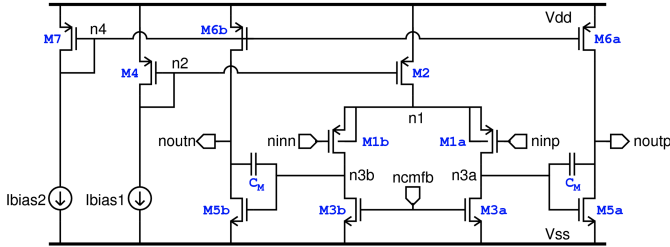


Figure 3. Sample schematics of the OPAMP to be designed.

III. RESULTS

A. Performance in homework type assessments

The aforementioned prompting algorithm, designed to clarify the problem statement without "hinting" the LLM has been utilised to solve regular analog/mixed-signal design homework-style questions. This approach allows the Claude 3.5 Sonnet LLM to achieve an average score of $\mu = 75.8\%$ and $\sigma = 36.5\%$, while solving assignments of varying difficulty across multiple domains typically covered in their corresponding courses. The breakdown of results is outlined in the Table IV. From more detailed results outlined in Tables I-III it becomes apparent that Claude 3.5 Sonnet mostly struggles with non-regular circuits and advanced problems, such as frequency response, noise and mismatch analysis.

Overall, it is clearly demonstrated that the publicly available LLM Claude 3.5 Sonnet is capable of performing circuit analysis and solving most of the easy and medium difficulty problems in circuit theory classes, adding another potential

source of academic integrity breaches, which may compromise the value of education provided.

B. OPAMP Netlisting and optimisation

The resulting LTspice netlist produced by Claude 3.5 Sonnet for the circuit shown in Figure 3 is indeed consistent with the schematic and as shown in Figure 4. This task was completed by Claude 3.5 Sonnet in 2 prompts, where the second prompt was used to correct the erroneous image processing of Claude 3.5 Sonnet. It must be noted, that Claude 3.5 Sonnet is also capable of providing correct instructions on how to use other design environments such as KiCAD and CADENCE Virtuoso to approach similar tasks.

When approaching the optimisation problem, the LLM was able to draw clear analytical relationships between small signal parameters and circuit specifications, except for forgetting to include Miller effect into dominant pole calculation and losing the 2π factor in phase margin expression, as can be seen from Table V. Notice that the error due to the Miller effect is consistent with the results in Table II. Afterwards, Claude was able to correctly use these numerical relationships and approximate gm/Id design with the EKV CMOS model to estimate the sizing of the transistors needed to meet the specifications.

The performance of the resulting LLM design and human expert design is compared in Table VI. It must be noted, that even though it might seem like Claude 3.5 has only been able to meet the gain-bandwidth product (GBW) specification the only mistake made was the sizing of the input differential pair. This, after quick adjustment, is capable of meeting the required specification, while using a minimal amount of power.

Table II.
SUMMARY OF MEDIUM PROBLEMS ATTEMPTED BY CLAUDE 3.5 SONNET

Problem	Technical Topic and Task	Domain	Grade	Comments
Medium Problems				
2.6 [7]	Sketch I_D and g_m as a function of external voltage	AC DC	A	✓ Correct I_D calculation. ✓ Correct g_m calculation.
2.13 [7]	Derive a gain-bandwidth (GBW) relationship	AC	A	✓ Determined GBW of common-source amplifier (CS) from small-signal parameters (SS) and parasitic capacitors. ✓ Converted GBW to transistor parameters.
3.21 (f,h) [7]	Small Signal Analysis of amplifiers with feedback	AC	A	✓ Successful at determining the small signal gain. ✓ Can analyse small circuits with feedback.
4.23 [8]	Maximum clock frequency given delays and optimized path delay.	Digital	A	✓ Correct maximum clock frequency. ✓ Correct assessment of impact of optimization.
4.4 [7]	Differential pair analysis	AC DC	A	✓ Successfully found saturation limits. ✓ Correct small signal gain at the given OP.
4.5 [7]	Differential pair analysis	AC DC	A	✓ Analysed the nature of current steering. ✓ Determined the operating point of the differential pair. ✓ Found SS parameters from OP.
7.1 [8]	Endian mismatch in dual-processor data sharing explanation and solutions.	Digital	A	✓ Correctly identified issue at hand. ✓ Correctly identified potential solutions to issue in question.
7.11 [8]	Embedded assembly programming for fictional 8-bit CPU	Digital	A	✓ Wrote correct, efficient ASM to accomplish requested task.
7.12a [7]	Noise in OTA	Noise	A	✓ Correct analysis.
8.14 [9]	Sampling noise	Noise	A	✓ Sampled noise estimate is correct.
9.14 [9]	FM sampling	AC	A	✓ SNR calculations are correct. ✓ Correct use of oversampling.
11.8 [9]	Linearity analysis of resistive ladder DAC	Linearity	A	✓ Correct integral/differential non-linearity (INL/DNL) analysis.
11.10 [9]	Distortion of current steering DAC	Linearity	A	✓ Correct INL/DNL analysis.
11.11 [9]	Linearity analysis of resistive ladder DAC	Linearity Mismatch	A	✓ Correct INL/DNL analysis. ✓ Correct total harmonic distortion (THD) analysis.
8.18 [9]	Track&Hold circuit SNR	AC	A	✓ Most of SNR calculations are correct. × Small error when adding different sources of noise.
13.6 [9]	Kickback noise in flash ADC	AC	B	✓ Mostly correct analysis of kickback noise in flash ADC. × Not the most accurate estimate of parasitic capacitance size.
2.28/2.29 [8]	Boolean equations, diagram, Verilog for BCD Decoder	Digital	B	✓ Correct Boolean Equations × Created poor diagram. ✓ Correct Verilog Implementation.
6.3 [7]	Frequency response of CS amplifier	AC	B	× Failed to apply Miller theorem to find input pole. ✓ Found output pole. ✓ Found zero.
9.15 [9]	Effective number of bits (ENOB) of ADC	Noise	B	✓ ENOB calculations are mostly correct. × Forgot thermal noise.
12.6 [9]	Kickback noise in flash ADC	AC	B	✓ Correct analysis of kickback noise. × Small error in determining the number of bits in flash ADC.
13.7 [9]	ENOB in flash ADC	AC Mismatch	B	✓ Correct estimate of ENOB in flash ADC due to clock jitter and mismatch of comparators.
3.61 [8]	Verilog entity declaration for squaring module	Digital	F	× Incorrect bit width on outputs. × Failed to follow good practice for fixed-point wires.
3.22/3.23 [8]	Verilog adder and testbench	Digital	F	× Misinterpreted request for no explicit overflow detection to mean no internal carry. ✓ Testbench checks core functionality, finds error in module. × Testbench does not check boundary conditions behaviour on all input settings.
6.2 [9]	Capacitor mismatch	Mismatch	F	× Mismatch calculation for capacitor due to perimeter variation is invalid.
7.16 [9]	Spectrum and sampling	AC	F	× Failed to determine relationship between spectrum before and after sampling.

Table III.
SUMMARY OF HARDER PROBLEMS ATTEMPTED BY CLAUDE 3.5 SONNET

Problem	Technical Topic and Task	Domain	Grade	Comments
Harder Problems				
6.16 [7]	Find poles and zeros in current amplifying OPAMP	AC	A	✓ Successfully found poles in differential OPAMP. ✓ Successfully found zeros in differential OPAMP.
4.22 [7]	Defective differential pair analysis	AC	B	✓ Correct differential gain. ✓ Correct CM gain. ✓ Correct CMRR of defective circuit. × Didn't ignore channel length modulation and produced incorrect result first time.
4.7 [8]	Synchronous Verilog peak detector with testbench	Digital	B	✓ Correct peak detector design. ✓ Testbench checks core functionality. × Testbench does not check boundary conditions behaviour on all input settings.
6.17 [7]	OPAMP phase shift analysis	AC	C	✓ Good theoretical reasoning. × Struggled to implement of 135° phase shift.
7.7 [7]	Noise analysis in different amplifiers	Noise	D	✓ Correct analysis of simpler topologies. × Struggled with more complex topologies.
3.25 [7]	Analysis of CS amplifier with triode load	AC DC	F	× Struggled to understand the idea behind the triode load. × Produced an incorrect analysis. × Confused g_m and g_{ds} .
6.9 (c,d) [7]	Low and high frequency response of non-standard amplifiers	AC	F	× Low frequency analysis fail. × High frequency analysis fail.

Table IV.
SUMMARY OF GRADES ACHIEVED BY CLAUDE 3.5 SONNET

	A	B	C	D	F
Digital	4	2	1	0	2
AC	14	4	1	0	3
DC	6	0	1	0	1
Mismatch	2	2	0	0	1
Linearity	3	0	0	0	0
Noise	3	2	0	1	0
Transient	1	0	0	0	0
Easy Problems	11	1	2	0	0
Medium Problems	15	6	0	0	4
Hard Problems	1	2	1	1	2

Table V.
NUMERICAL RELATIONSHIPS IN OPAMP

Parameter	Claude 3.5 Sonnet	Actual Expression
Gain (V/V)	$(g_{m1}(r_{o1} \parallel r_{o3})) \bullet (g_{m5}(r_{o5} \parallel r_{o6}))$	$(g_{m1}(r_{o1} \parallel r_{o3})) \bullet (g_{m5}(r_{o5} \parallel r_{o6}))$
GBW (MHz)	$g_{m1}/(2\pi C_m)$	$g_{m1}/(2\pi C_m)$
Dominant Pole ω_d	$\frac{1}{(r_{o1} \parallel r_{o3})} C_m$	$\frac{1}{g_{m5}(r_{o5} \parallel r_{o6})(r_{o1} \parallel r_{o3})} C_m$
Non-dominant Pole ω_{nd}	g_{m5}/C_L	g_{m5}/C_L
PM (°)	$90^\circ - \text{atan}(\frac{GBW}{\omega_{nd}})$	$90^\circ - \text{atan}(\frac{2\pi GBW}{\omega_{nd}})$
Slew Rate (V/ μ s)	$\min(I_2/C_m, I_6/C_L)$	$\min(I_2/C_m, I_6/C_L)$

This could easily be discovered by a student with minimal experience, simply by looking at the operating point of the circuit, or performing a few parametric sweeps.

This clearly shows that LLMs today are capable of assisting students in both learning design tools and tackling complex design projects, adding another potential source of academic integrity violation and potentially compromising the value of education provided.

Table VI.
PERFORMANCE OF OPAMP DESIGNED BY DIFFERENT AGENTS

Parameter	Specification	Claude 3.5 Sonnet	Claude 3.5 Sonnet + Human Expert
Design Time	-	2 prompts	2 prompts + 10 minutes
Gain (V/V)	>2000	533	2750
GBW (MHz)	>120	240	169
PM (°)	>45	-40	45
Core Power (mW)	minimise	2.556	2.61
Slew Rate (V/ μ s)	>150	375	400

IV. DISCUSSIONS

A. Principal Findings

From the above results, it becomes apparent that the latest generation of publicly available LLMs, such as Claude 3.5 Sonnet, can create a breach of academic integrity in the continuous assessment component of electronic engineering courses, particularly those on digital design, analog design, mixed-signal design and signal processing. While not quite keeping up with the latest developments in other engineering domains, the emergent capabilities here are consistent with the increasing capabilities of LLMs in RTL development [10] and software engineering [11].

With the LLM scoring around 76% on average in homework-style assignments, it can match the performance of an average student, with the obtained percentage being representative of B-level grades or higher in most modern educational institutions. It must be noted, that it does begin to struggle when facing unusual multi-transistor circuits and complex topics such as frequency response or noise analysis. There is undoubtedly room for improvement here, however, with more specialised AI models potentially emerging[12]. Moreover, delving into these advanced concepts may not be relevant in beginner courses, where students are only getting familiarised with basic transistor operation. This suggests that the academic integrity of take-home homework will soon be endangered by AI.

```

* Two-stage Fully Differential Operational
Amplifier
* TSMC 180nm process

* Models (simplified for LTspice compatibility)
.model CMOSN NMOS (LEVEL=8 VERSION=3.1 TOX=4.1E-9
VTH0=0.3662473 K1=0.5864999 U0=273.8094484
VSAT=1.355009E5)
.model CMOSP PMOS (LEVEL=8 VERSION=3.1 TOX=4.1E-9
VTH0=-0.3906012 K1=0.5341312 U0=115.6894042
VSAT=1.130982E5)
* Circuit netlist
M1a n3a ninp n1 Vdd CMOSP W=40.5u L=300n M=1
M1b n3b ninn n1 Vdd CMOSP W=40.5u L=300n M=1
M2 n1 n2 Vdd Vdd CMOSP W=57u L=200n M=1
M3a n3a ncmfb Vss Vss CMOSN W=21.5u L=1000n M=1
M3b n3b ncmfb Vss Vss CMOSN W=21.5u L=1000n M=1
M4 n2 n2 Vdd Vdd CMOSP W=57u L=200n M=1

M5a noutp n3a Vss Vss CMOSN W=96u L=200n M=1
M5b noutn n3b Vss Vss CMOSN W=96u L=200n M=1
M6a noutp n4 Vdd Vdd CMOSP W=96u L=200n M=1
M6b noutn n4 Vdd Vdd CMOSP W=96u L=200n M=1
M7 n4 n4 Vdd Vdd CMOSP W=48u L=200n M=1

* Compensation capacitors
CM1 nc1 n3b 500f
CM2 nc2 n3a 500f
RM1 nc1 noutp 300
RM2 nc2 noutn 300

* Bias current sources
Ibias1 n2 Vdd DC 50u
Ibias2 n4 Vdd DC 400u

* Power supplies
Vdd Vdd 0 DC 1.8
Vss 0 Vss DC 0

* Common-mode feedback (simplified)
Ecmfb ncmfb 0 VALUE=1.3-(V(noutp)+V(noutn))/2

* Input voltage sources for testing
Vinp ninp 0 AC 0.5 DC 0.9
Vinp ninp 0 SINE(0.9 10u 100)
Vinn ninn 0 AC -0.5 DC 0.9
* Load capacitors
CL1 noutp 0 2p
CL2 noutn 0 2p

```

Figure 4. Netlist of the OPAMP produced by Claude 3.5 Sonnet

The same applies to projects, such as OPAMP design, which can be largely assisted by state-of-the-art LLMs demonstrably capable of basic circuit analysis and optimisation. The models also provide relatively good reasoning which could be used as the basis for design reports. This poses a large threat not only to assessment but also to the educational aspect of the engineering course, where big projects are used to foster creative thinking and develop students' practical skills on real-world examples [13].

The argument could be made that using AI is not particularly different from copying assignments from a particularly capable study partner, with the common opinion being that students already cross-collaborate inappropriately on take-home assignments [14]. However, the instant presence of such a capable LLM agent makes the act of cheating a lot easier, while reducing the probability of plagiarism.[15] A student

can use such parameters as temperature to make LLMs more creative[16] or feed their LLM of choice with their own previous reports, prompting the model to match the style and tone of the completed coursework.

If students use these LLM agents instead of attempting the problems themselves, their fundamental knowledge will suffer, which in turn will limit their ability to solve more complex problems. Potentially, this can cause a massive decline in the amount and quality of knowledge absorbed and an increased failure rate for cheating students [17]. This is obviously an inefficient use of time for both students and lecturers, hence, something needs to be done to mitigate this issue.

At the same time, it is obvious that an LLM such as Claude 3.5 Sonnet can perform the function of a teaching assistant [17], [18], helping students to understand more advanced topics within engineering. As such, it would also not be correct to completely eliminate AI out of the educational process.

B. Proposed Framework

The issue imposed by breaches in homework can be solved by adding more creative problems into homework assignments mixed with continuous closed-book examination [14], with the goal of encouraging students to be more involved in the educational process and eliminating classical sources of breaches in academic integrity such as copying from a study partner.

We also propose a similar approach for project/lab-based learning. Here, at the end of the module, a practical exam should be held, testing the ability of students to utilise the new knowledge/tools on practical tasks in a limited amount of time. This should be conducted in a controlled environment where the use of AI tools is actively monitored by invigilators or limited by some form of firewall. The problem complexity has to be correspondingly reduced, for instance, instead of a differential 2-stage OPAMP shown in Fig. 3, a 5-transistor OTA would be designed and briefly documented during the exam slot.

The suggested practical exams would encourage students to actively engage in continuous assessment, while allowing to adequately assess the practical skills they learned during the course. A similar technique can be adopted for any module that has a heavy practical component, ranging from software engineering and modelling to circuit design modules that require specific CAD tools. Additionally, the weighting of in-person assessments should increase, therefore, limiting the impact of LLMs on the final grade of the student.

Overall, this approach in assessment allows for the utilization of the benefits of LLMs acting as individual TAs for continuous assessment while minimising their impact on the assessment, and maintaining a high standard of engineering education.

V. CONCLUSIONS

The study presents an extensive view into the capabilities of state-of-the-art LLMs when applied to circuit design problems and projects frequently encountered in education. It seems very plausible that in the near future, LLMs can compromise the continuous assessment section of circuit design modules. This paper proposes a sensible approach on how to mitigate this issue and ensure that the quality of education remains at the same standard, while remaining permissive of students using LLMs to gain additional insight into course material.

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